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Key Steps to Design a Post-regulator Driven by the NCP4331

Prepared by: Joël Turchi,
ON Semiconductor

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This paper proposes the key steps to rapidly design a post regulator driven by the NCP4331, in a systematic manner. The process is illustrated by a practical 3V3 / 20 A design where the post regulator is coupled to a power supply operating at 70 kHz.

INTRODUCTION

There exist converters able to provide several output voltages as required in ATX applications for instance. However, they cannot tightly regulate all the outputs. Further regulating some of them by the way of dc−dc regulator or low drop regulators is not an efficient option. That is why, the so−called Secondary Side Post Regulators (SSPR) are often ideal in multi−outputs applications where efficiency and compactness are key requirements. Among them, magnetic amplifier solutions (mag amp) are very popular in PC power supplies.

Coupled to a main power supply, the global solution operates as follows:

- The highest output is traditionally regulated by the regulation means of the main converter. The converter duty ratio is modulated accordingly.
- The SSPR post−regulates the other ones, ***by directly drawing the energy from the transformer secondary ac voltage.***

Conduction losses are the major limitation of this solution because of the ohmic dissipation in the magnetic component (the mag amp itself that gave the name of this structure) and in the two diodes that conduct the current.

NCP4331 driven post−regulators represents a major leap towards efficiency. Like mag amp, they can be viewed as buck converters with the ability to operate from a pulsed input voltage. However, NCP4331 driven post−regulators dramatically improves the efficiency of the power processing as:

- The conduction losses are significantly reduced since the mag amp is removed and since the diodes are replaced by low $R_{ds(on)}$ N−MOSFETs (synchronous rectification)
- The switching losses are minimized since three out of the four switching transitions of the MOSFETs are soft thanks to a smart sequencing.

Typically, they are associated to forward converters as portrayed by Figure 1.

One can associate the NCP4331 to other architectures (like 2−switch forward, active clamp forward or half bridge converters). As a matter of fact, any converter able to provide the NCP4331 post−regulator with a square wave source can use this concept (Note 1).

Also, the NCP4331 incorporates all the functions necessary for a reliable post−regulation.

In particular, it embeds powerful features to protect the application from possible over−stresses and make the post−regulator very rugged. A second operational amplifier is available to lower the duty−ratio and ultimately clamp the output current when it tends to become excessive (Constant Current Constant Voltage characteristic). Also, the soft−start and the under−voltage protections improve reliability and in addition, they help control the start and stop sequencings. Ultimately, the integration within the whole system is eased.

Post Regulation Operation

Figure 1 illustrates the concept where two outputs are to be regulated ("V_{out1}" and "V_{out2}"). For the sake of the simplicity, the forward converter of Figure 1 consists of a simple demagnetization winding and of output diodes, but more sophisticated options including active clamp and synchronous rectification, would lead to a better global efficiency of the solution.

The highest output (V_{out1}) is directly regulated by the way of a traditional regulation arrangement that typically consists of a TL431 and an opto−coupler. This regulation arrangement modulates the forward converter duty ratio. The other output (V_{out2}) is regulated by a dual MOSFET arrangement driven by the NCP4331. The high−side MOSFET turns on during one part of the forward converter on−time, while the low−side power switch is ON for the rest of the period (free wheeling).

1. As long as the NCP4331 maximum ratings are not exceeded (in particular, the "BST" and "HB" maximum voltage)

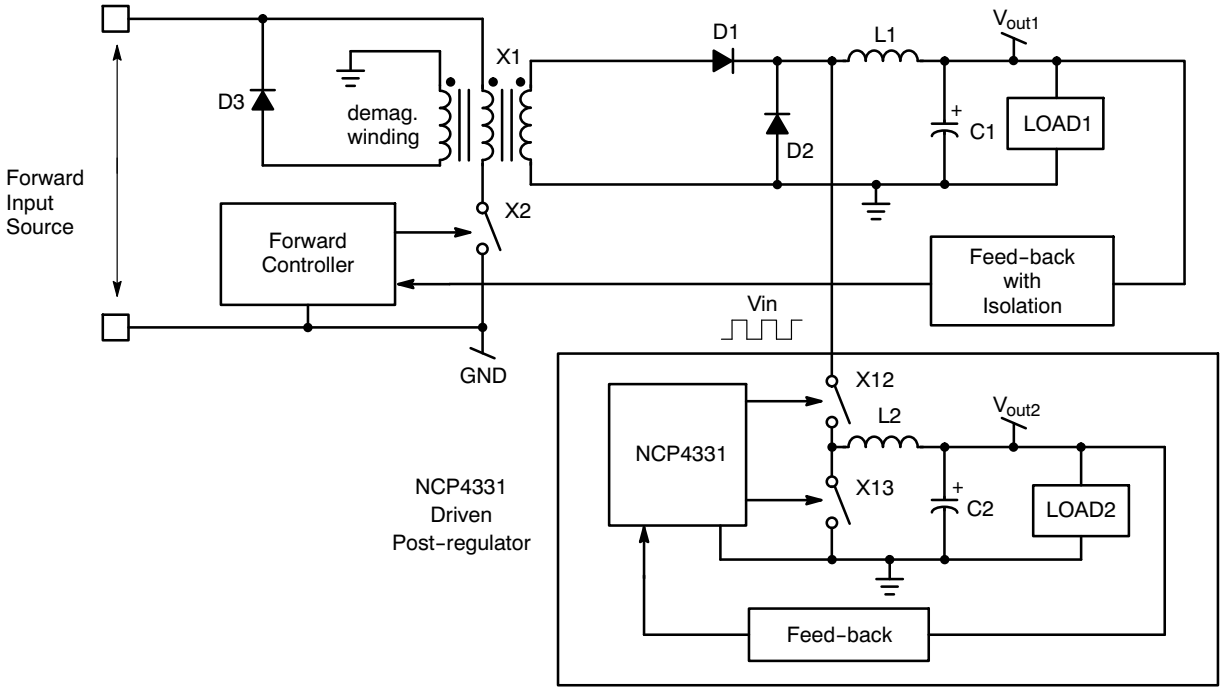

Figure 1. NCP4331 Post−regulator Associated to a Forward Converter

In the case of a forward converter operating in continuous conduction mode (CCM) operation, the duty ratio is simply given by the following equation (the converter losses being neglected):

$$d_f = \frac{V_{out1}}{\frac{N_S}{N_P} \cdot (V_{in})_{forward}}$$

where:

- N_S/N_P is the transformer turn ratio (N_P: primary number of turns, N_S: secondary number of turns),
- $(V_{in})_{forward}$ is the forward converter input voltage,
- V_{out1} is the main output voltage of the forward converter.
- d_f is the duty ratio of the forward converter

The post−regulator input voltage (V_{in}) is : $\frac{N_S}{N_P} \cdot (V_{in})_{forward}$ during the on−time of the forward converter

- Zero otherwise since D_2 of Figure 1 is on (free wheeling phase) in CCM operation

As in a traditional buck converter, if the losses are neglected, the post−regulated output voltage is given by the following equation:

$$V_{out} = d \cdot \frac{N_S}{N_P} \cdot (V_{in})_{forward}$$

where: d is the duty ratio of the post−regulator.

The input voltage (V_{in}) is only able to provide energy when high, that is, during the forward converter on−time. Hence, the effective on−time of the post−regulator cannot be longer than ($d_f \cdot T_{SW}$) where T_{SW} is the switching period.

In other words, the duty−ratio of the post−regulator cannot exceed that of the main converter: ($d < d_f$). That is why post−regulated output voltages are necessarily lower than the main regulated one. However, the NCP4331 scheme allows d to nearly equate d_f so that if necessary, a post−regulated output voltage can be very close to the main one (V_{out1}).

Figure 2 details the way the post−regulator duty−ratio is adjusted.

The post−regulator controls the energy absorbed from the pulsed power source V_{in} by dictating the time during which the high−side MOSFET is on. Practically, the leading edge of the high side drive is modulated accordingly while the trailing edge is synchronized to that of the input voltage V_{in}.

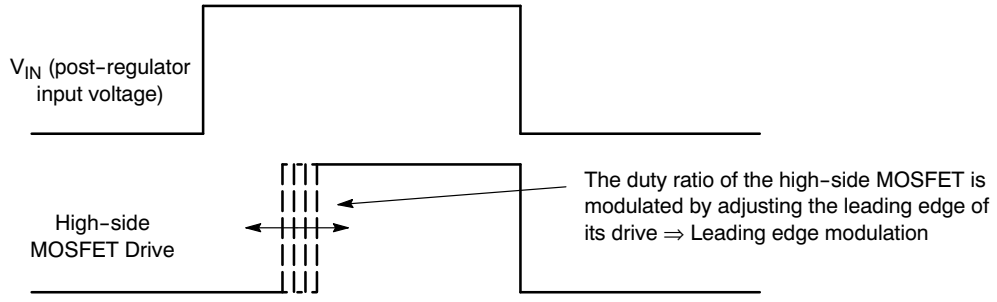

Figure 2. Leading Edge Modulation

Dimensioning of the Post−regulator

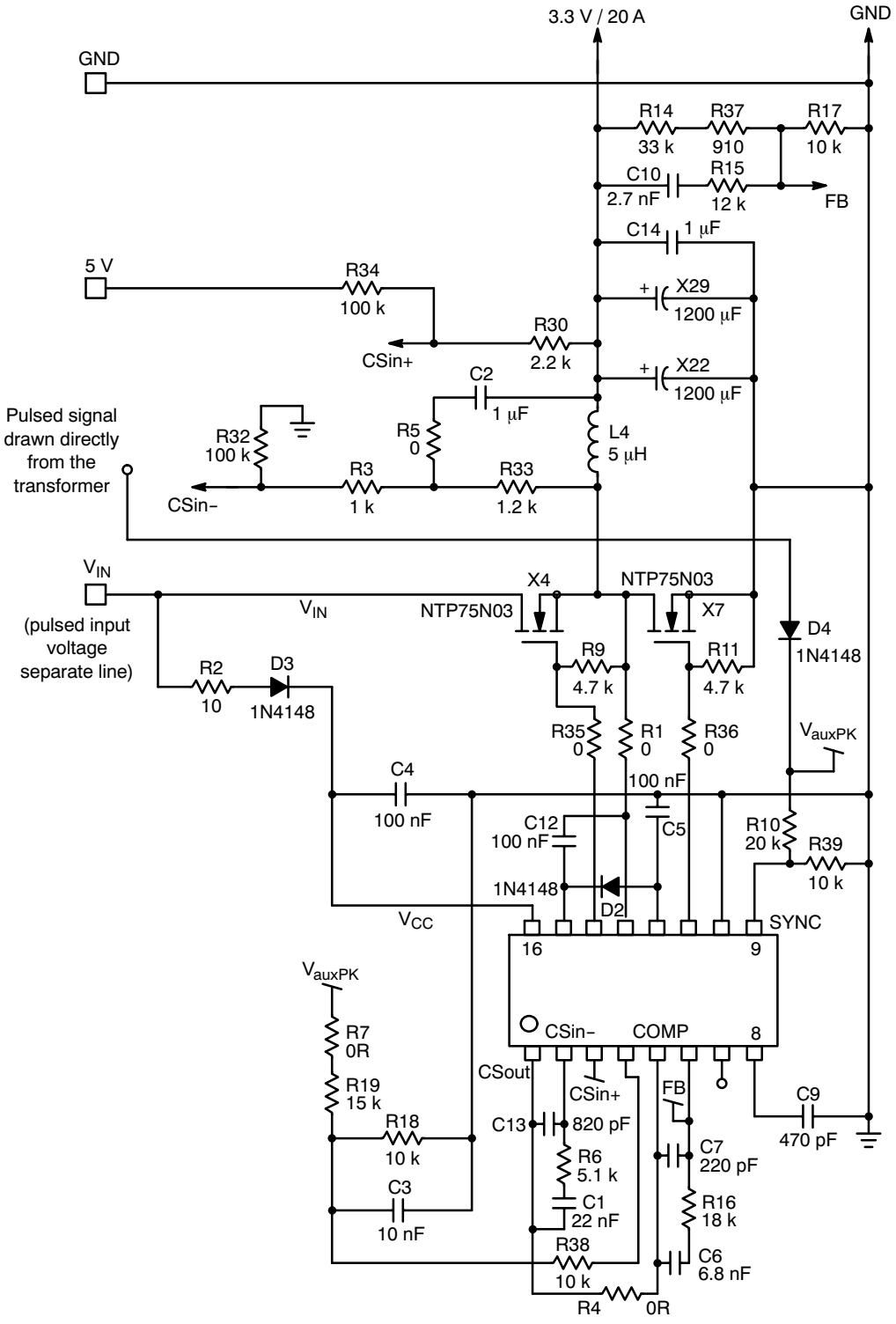

Figure 3. Application Schematic

Step 1 – Power Components Selection

Basically, the inductor, the bulk capacitor and the power MOSFETs are dimensioned as in any buck converter. This chapter does not detail all steps in very deep details, but provides a process and the main design criteria for an efficient a rapid implementation of your post−regulator.

Output Filter Selection

The output filter formed by the output coil and the bulk capacitor, averages the pulsed signal applied to the HB node to form V_{out}. The resonant frequency must be selected low enough to properly attenuate the output voltage ripple.

Practically, the bulk capacitor is dimensioned as a function of its ability to limit the output under/overshoot under load step. Hence, the maximum permissible deviation from the regulation level dictates its specification.

As for the inductor, designers of bulk converters often have to select it large enough to maintain continuous conduction mode operation (CCM) over the full power range. The goal is to keep the same function transfer that would otherwise change when in light load, the system enters discontinuous conduction mode. Since the NCP4331 permanently operates in CCM, including in no load conditions (see data sheet for more information), this criterion is no more relevant. Instead, we simply have to select the inductor so that the output filter resonant frequency

$$\left(\frac{1}{2\pi \cdot \sqrt{L \cdot C_{bulk}}}\right)$$

is low enough for a proper limitation of the output switching ripple.

Selecting the Buck Capacitor

The bulk capacitor limits the output voltage variations in case of load step according to the following (approximate) equation:

$$\Delta V_{out} = \left(\frac{1}{2\pi \cdot f_c \cdot C_{bulk}} + r_c\right) \cdot \Delta I_{out} \qquad \text{(eq. 1)}$$

Where:

- ΔI_{out} is the load current step
- ΔV_{out} is the V_{out} variation resulting from ΔI_{out}
- f_c is the cross−over frequency (10 kHz in our application)
- C_{bulk} is the capacitance of the bulk capacitor
- r_c is the series resistor of the bulk capacitor (ESR).

If a maximum 165 mV voltage drop is allowed when a 6 A load step is applied, as a rule of the thumb, we can devote 75% of this drop in the ESR, the rest being the capacitive drop.

$$\text{Hence: } C_{bulk} \geq \frac{\Delta I_{out}}{2\pi \cdot f_c \cdot 25\% \cdot \Delta V_{out}} = \frac{6}{2\pi \cdot 10\,k \cdot 25\% \cdot 165\,m} \cong 2.32\,mF \qquad \text{(eq. 2)}$$

$$r_c \leq \frac{75\% \cdot \Delta V_{out}}{\Delta I_{out}} = \frac{75\% \cdot 165\,m}{6} \cong 21\,m\Omega \qquad \text{(eq. 3)}$$

Two paralleled 1200 μF / 6.3 V capacitors (Panasonic FM series, ref. EEUFMOJ122L) are used for a total 2.4 mF capacitance featuring a global ESR equal to 13 mΩ at 20°C.

A 1 μF ceramic capacitor is placed in parallel to the bulk capacitors to further filter the switching noise and in particular that produced by the parasitic inductor of the bulk capacitor (ESL) (Note 2).

Selecting the Inductor

The coil inductance adjusts the ripple of the coil current and ultimately, the output voltage ripple together with the bulk capacitor.

Approximating the duty ratio to its value in a 100% efficiency bulk converter $\left(d = \frac{V_{out}}{V_{in}}\right)$

the current ripple in the inductor is:

$$(\Delta I_{out})_{pk-pk} = \frac{(V_{in} - V_{out}) \cdot V_{out}}{L \cdot f_{SW} \cdot V_{in}} \qquad \text{(eq. 4)}$$

The output voltage ripple can be split into two components both linked to the current ripple:

Capacitive ripple:

$$(\Delta V_{out})_{pk-pk} = \frac{(\Delta I_{out})_{pk-pk}}{8 \cdot C_{bulk} \cdot f_{SW}} \qquad \text{(eq. 5)}$$

Ripple due to the ESR:

$$(\Delta V_{out})_{pk-pk} = r_c \cdot (\Delta I_{out})_{pk-pk} \qquad \text{(eq. 6)}$$

As shown in Figure 4, the two ripple components do not peak simultaneously (Note 3). However, since often, the resistive part is largely predominant, summing the two contents generally give a value a bit conservative but precise enough of the global ripple.

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2. The ESL role was not detailed in this section for the sake of simplicity.
3. One can show that the maximum ripple is obtained at: $t_{rmax} = t_{on}$ if $t_{off} - (2 \cdot r_c \cdot C_{bulk}) < 0$. Otherwise, $t_{rmax} = t_{on} + t_{off}/2 - (r_c \cdot C_{bulk})$

and that: $(\Delta V_{out})_{pk-pk} = \frac{r_c \cdot (\Delta I_{out})_{pk-pk}}{2} \cdot \left(1 - \frac{2 \cdot t_{rmax}}{t_{off}}\right) + \frac{(\Delta I_{out})_{pk-pk}}{2 \cdot C_{bulk}} \cdot \left(t_{rmax} - \frac{t_{rmax}^2}{t_{off}}\right)$

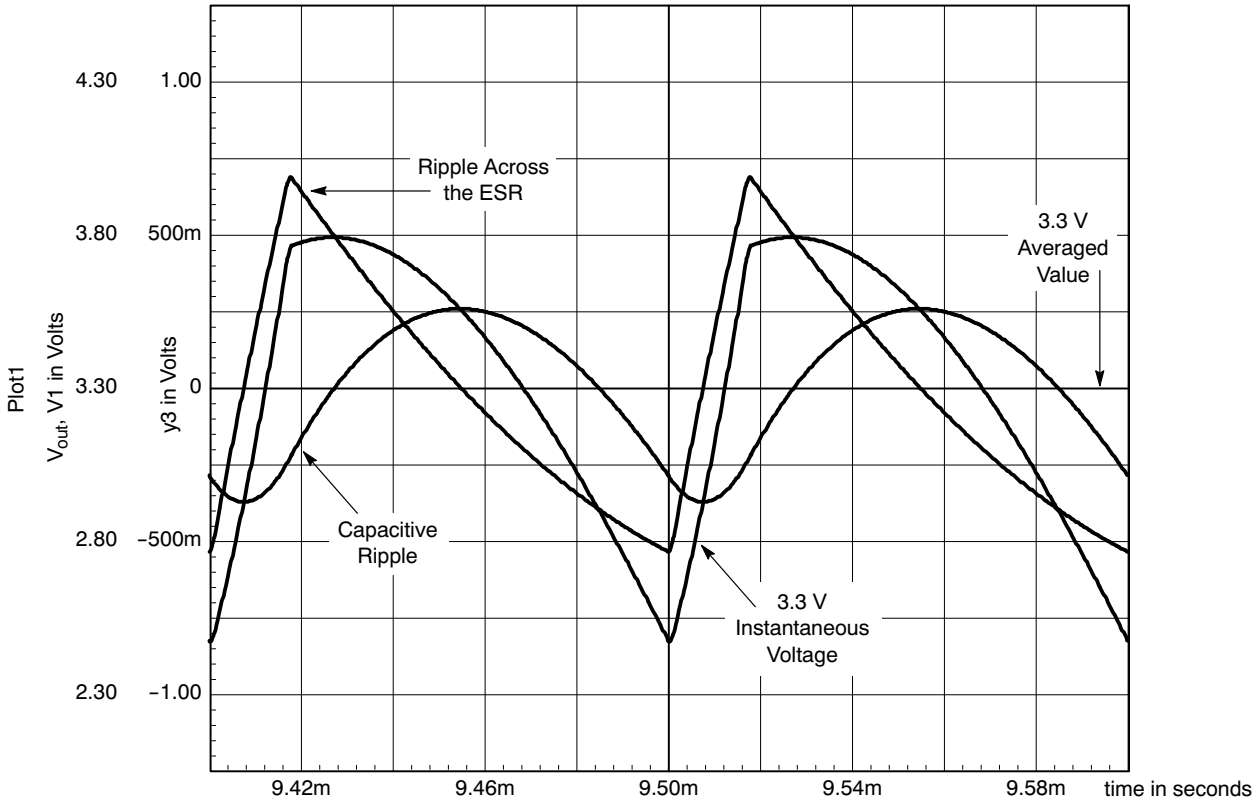

Figure 4. Capacitive and Resistive Components of the Output Voltage Ripple
(simulations results obtained with a 100 mF capacitor exhibiting a 25 mW ESR)

Doing so, the global output voltage ripple is: $(\Delta V_{out})_{pk-pk} = \left(r_c + \frac{1}{8 \cdot C_{bulk} \cdot f_{SW}}\right) \cdot (\Delta I_{out})_{pk-pk}$ (eq. 7)

Knowing the maximum permissible ripple on the output voltage, one can deduce the maximum coil current ripple and ultimately, the minimum inductor value.

For instance, if this peak to peak ripple is specified to be below 165 mV ($(\Delta V_{out})_{pk-pk} \leq 165$ mV), we have:

$$(\Delta I_{out})_{pk-pk} \leq \frac{165\ m}{\left(r_c + \frac{1}{8 \cdot C_{bulk} \cdot f_{SW}}\right)} = \frac{165\ m}{\left(13\ m + \frac{1}{8 \cdot 2.4\ m \cdot 70\ k}\right)} \cong 12\ A \quad \text{(eq. 8)}$$

$$\text{and: } L \geq \frac{(V_{in} - V_{out}) \cdot V_{out}}{(\Delta I_{out})_{pk-pk} \cdot f_{SW} \cdot V_{in}} = \frac{(20 - 3.3) \cdot 3.3}{12 \cdot 70\ k \cdot 20} \cong 3.28\ \mu H \quad \text{(eq. 9)}$$

The coil with part number 86A−7092 (Delta Electronics) is selected that exhibits an inductance of 5.2 μH @ 0 A and 4.5 μH @ 25 A. Its series resistance is 4.7 mΩ maximum.

Attention Points Regarding the Above Selection:

- Resonant frequency: The selected components lead to the following resonant frequency:

$$\frac{1}{2\pi \cdot \sqrt{L \cdot C_{bulk}}} = \frac{1}{2\pi \cdot \sqrt{5\ \mu \cdot 2.4\ m}} \cong 1.4\ kHz \quad \text{(eq. 10)}$$

This frequency is well below the switching frequency, as necessary. Practically, it should be at least 15 times lower than the switching frequency. Here, the ratio is high enough since

$$\left(\frac{70\ kHz}{1.4\ kHz} = 50 \geq 15\right)$$

If it was not the case, we should have to increase C_{bulk} to obtain a sufficient ratio (Note 4).

4. Otherwise, when closing the loop, it is difficult to properly place a crossover frequency (see “Step 3”).

- Inductance conduction losses:
  The current ripple in the inductor is:

$$(\Delta I_{out})_{pk-pk} = \frac{(20 - 3.3) \cdot \frac{3.3}{20}}{4.5\ \mu \cdot 70\ k} = 8.7\ A \quad \text{(eq. 11)}$$

The RMS value of the coil current is the quadratic sum of the dc and ac contents:

$$I_{L(rms)} = \sqrt{I_{L(dc)}^2 + I_{L(ac)}^2} = \sqrt{I_{out}^2 + \left(\frac{(\Delta I_{out})_{pk-pk}}{2}\right)^2} \quad \text{(eq. 12)}$$

The conduction losses due to the series resistor (r_L) can then be computed by the following equation:

$$P_{r_L} = r_L \cdot \left(I_{out}^2 + \frac{(\Delta I_{out})_{pk-pk}^2}{12}\right) \quad \text{(eq. 13)}$$

Hence, since our inductance exhibits 4.7 mΩ max, the ohmic losses are:

$$P_{r_L} \leq 4.7\ m \cdot \left(20^2 + \frac{8.7^2}{12}\right) = 1.9\ W \quad \text{(eq. 14)}$$

- Final output ripple:
  Our final output voltage ripple is:

$$(\Delta V_{out})_{pk-pk} = \left(r_c + \frac{1}{8 \cdot C_{bulk} \cdot f_{SW}}\right) \cdot (\Delta I_{out})_{pk-pk} = \left(13\ m + \frac{1}{8 \cdot 2.4\ m \cdot 70\ k}\right) \cdot 8.7 \cong 120\ mV \quad \text{(eq. 15)}$$

- Conduction losses in the bulk capacitor
  The current that flows through the capacitor is the ac content of the coil one. Hence the capacitor rms current is:

$$I_{c,rms} = \frac{(\Delta I_{out})_{pk-pk}}{\sqrt{12}}$$

that leads to the following losses:

$$r_c \cdot I_{c,rms}^2 = r_c \cdot \frac{(\Delta I_{out})_{pk-pk}^2}{12} = 13\ m \cdot \frac{8.7^2}{12} \cong 82\ mW \quad \text{(eq. 16)}$$

MOSFETs

The two MOSFETs derive the whole coil current. In a first approach, the switching losses can be neglected since the NCP4331 offers three soft switching transitions out of four (see data sheet for more information). The main losses are then the conduction ones.

If $R_{DS(on)1}$ is the drain−source on−time resistor of the high−side MOSFET and if $R_{DS(on)2}$ is that of the low−side one:

$$P_M = \left\{R_{DS(on)1} \cdot \left(I_{out}^2 + \frac{(\Delta I_{out})_{pk-pk}^2}{12}\right) \cdot d\right\} + \left\{R_{DS(on)2} \cdot \left(I_{out}^2 + \frac{(\Delta I_{out})_{pk-pk}^2}{12}\right) \cdot (1 - d)\right\} \quad \text{(eq. 17)}$$

In our application, the input and output voltages being 20 V and 3.3 V respectively, the duty−ratio d $\left(\cong \frac{V_{out}}{V_{in}}\right)$ is about 16.5%

Hence:
$$P_M = \left\{\left(0.165 \cdot R_{DS(on)1}\right) + \left(0.835 \cdot R_{DS(on)2}\right)\right\} \cdot \left(I_{out}^2 + \frac{(\Delta I_{out})_{pk-pk}^2}{12}\right) \quad \text{(eq. 18)}$$

As the load current can be as high as 20 A and since the peak to peak ripple of the coil current is 8.7 A:

$$P_M = \left\{\left(0.165 \cdot R_{DS(on)1}\right) + \left(0.835 \cdot R_{DS(on)2}\right)\right\} \cdot \left(20^2 + \frac{8.7^2}{12}\right) \cong \left(67 \cdot R_{DS(on)1}\right) + \left(339 \cdot R_{DS(on)2}\right) \quad \text{(eq. 19)}$$

The duty ratio d being low in the presented application, the stress on the high−side MOSFET is much smaller compared to that of the low−side. Hence, it can make sense to use a smaller MOSFET for the high−side. However, our demo−board being intended to be coupled to different possible converters (possibly with higher d), the same MOSFET was used in the two sides.

Practically, two NTP75N03 have been selected ($R_{DS(on)}$ = 10 mΩ):

$$p_M \cong (67 \cdot 10\ m) + (339 \cdot 10\ m) \cong 4\ W \quad \text{(eq. 20)}$$

Remark:

If instead of the two MOSFETs we would use two diodes featuring a similar Vf of 0.6 V, the losses would amount to:

$$p_{diodes} = (V_f \cdot I_{out} \cdot d) + \left(V_f \cdot I_{out} \cdot (1 - d)\right) = 0.6 \cdot 20 = 12\ W$$

Thanks to the NCP4331, about 8 W are saved!

Step 2 − Synchronization

As already mentioned, the NCP4331 operation is to be synchronized to the main converter. This section will then deal with the signal to apply to the synchronization pin but it will also include design recommendations regarding:

- The Under−Voltage Protection pin that is mainly intended to detect the absence of activity of the main converter. Its role is key to have a clean stop sequence.
- The capacitor to connect to the RAMP pin which swing is to be adapted to the switching frequency.

Preliminary question: which signal to synchronize the post-regulator?

Generally speaking, the input voltage is the obvious option. However, since this voltage is the vehicle for an important power transfer, it may be the seat of an important noise and the use of another signal can be beneficial.

Also, one can note that V_{in} is just separated from the main output V_{out1} by an inductor. Hence, when the main converter stops operating, V_{in} may stabilize to V_{out1} during its decay, leading to a long high signal to be applied to the synchronization pin during which the high−side MOSFET remains on. Ultimately, the post−regulator output can charge to V_{out1}.

That is why, it is recommended to use another signal. For instance, the voltage across the secondary winding of the transformer can be used through a diode in the case a 2−switch forward, (see Figure 5). If the 2−switch forward incorporates synchronous rectification, the drive signal of the free−wheeling MOSFET is another option for synchronization.

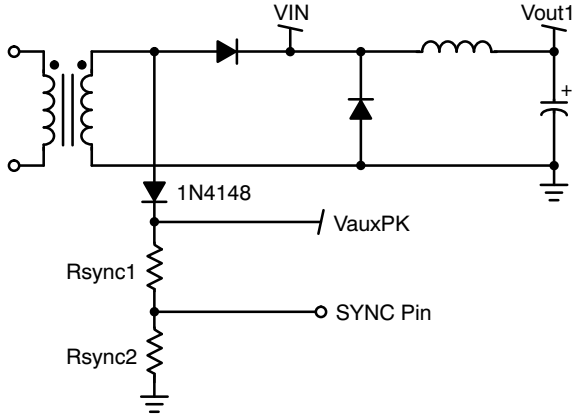

Figure 5. Synchronization Signal

Generally speaking, "V_{auxPK}" should be a signal very similar to V_{in} but "cleaner" since not distorted by the power transfer. Also, "V_{auxPK}" should drop to zero when the main converter stops operating.

In the rest of the document, we suppose that we use a signal "V_{auxPK}", wherever it is drawn from.

Synchronization Network:

The synchronization network should be selected so that a pulse higher than the internal threshold (2.6 V maximum) is applied to the SYNC pin during operation.

So, the resistor divider of figure (R_{sync1}, R_{sync2}) must meet the following constraint:

$$\frac{R_{sync2}}{R_{sync1} + R_{sync2}} \cdot (V_{auxPK})_{min} \geq 2.6\ V \qquad \text{(eq. 21)}$$

In other words:

$$R_{sync1} \leq \frac{(V_{auxPK})_{min} - 2.6\ V}{2.6\ V} \cdot R_{sync2} \qquad \text{(eq. 22)}$$

Assuming a 12 V minimum value for $(V_{auxPK})_{min}$, and if R_{sync2} is selected equal to 10 kΩ, one can deduce:

$$R_{sync1} \leq 3.6 \cdot 10\ k = 36\ k\Omega \qquad \text{(eq. 23)}$$

In our application, R_{sync1} = 22 kΩ is selected.

Note: the SYNC pin voltage being internally clamped, the R_{sync1} impedance must be high enough to limit the clamp current below 2 mA when the voltage on the synchronization pin is 5 V.

In other words:

$$R_{sync1} \geq \frac{(V_{auxPK})_{max} - 5\ V}{2\ mA} \qquad \text{(eq. 24)}$$

In our case, $(V_{auxPK})_{max}$ being 20 V, R_{sync1} must be higher than 7.5 kΩ. Our initial choice is then correct.

Selection of the C_{RAMP} Capacitor:

The RAMP capacitor must be selected:

1. High enough so that the ramp voltage does not reach the level necessary to turn on the high−side MOSFET at the end of a switching cycle. This is to get sure that the high−side duty−ratio is null when the error amplifier output is in low state (HS turns high when the sum (ramp + error amplifier output) exceeds the 3 V internal voltage reference V_{PWM}).
2. Low enough not to have an excessive loop gain.

Practically, let's calculate the lowest capacitor that can meet criterion 1. Practically, the voltage across C_{RAMP} that charges along each switching period with a current I_{RAMP}, must not reach the lowest voltage (V_{ramp}ON of the data sheet*)* that allows the HS MOSFET to turn on. To compute this minimum capacitance, we will take into account the dispersion of the RAMP parameters (as specified in the data sheet) and the switching period maximal value (worst case analysis).

Finally, C_{RAMP} must be chosen as follows:

$$C_{RAMP} \geq \frac{(I_{RAMP})_{max}}{(V_{RAMP}ON)_{min} \cdot (f_{SW})_{min}} = \frac{60\ \mu A}{2.3 \cdot (f_{SW})_{min}} \cong \frac{26\ \mu}{(f_{SW})_{min}} \qquad \text{(eq. 25)}$$

Where:

- $(I_{RAMP})_{max}$ is the maximum value of the RAMP current
- $(V_{RAMP}ON)_{min}$ is the minimum value required to have the high side on while the error amplifier output is low
- $(f_{SW})_{min}$ is the minimum value of the switching frequency.

In our 70 kHz application, we consider that the switching frequency can be as low as 63 kHz (±10 % spread). This leads to:

$$C_{RAMP} \geq \frac{26\ \mu}{63\ kHz} \cong 413\ pF \qquad \text{(eq. 26)}$$

A 470 pF capacitor is chosen.

Under Voltage Protection (UVP) Network:

The UVP pin is implemented for a rapid detection of the absence of activity of the main converter.

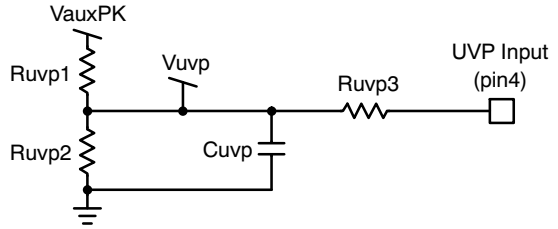

Figure 6. Circuitry for Under−Voltage Protection

Figure 6 gives an example of the circuitry that can be used for the under−voltage protection.

$V_{AUX}PK$ is the pulsed signal used for synchronization. A portion is integrated so that an averaged value of $V_{AUX}PK$ is obtained across C_{UVP}. This voltage must exceed the maximum internal threshold 2.2 V to allow operation. R_{uvp1} and R_{uvp2} must then be selected accordingly.

In our application, R_{uvp1} and R_{uvp2} are 15 kΩ and 10 kΩ respectively.

The capacitor C_{UVP} is selected to maintain a minimum inertia on the pin. This inertia should be as low as possible for a rapid detection of the START and STOP sequences of the main converter. As a rule of the thumb, one can set a time constant corresponding to 3 or 4 switching periods:

$$\left(R_{uvp1}//R_{uvp2}\right) \cdot C_{uvp} \cong \frac{4}{f_{SW}} \qquad \text{(eq. 27)}$$

In our application (f_{SW} =70 kHz), this leads to

$$\left(C_{uvp} = \frac{4}{6\ k \cdot 70\ k} \cong 9.5\ nF\right).\ 10\ nF \text{ is selected.}$$

The UVP internal comparator features a 60 mV hysteresis to avoid erratic detection. In addition, when no fault is detected, the UVP pin sources (I_{uvp} = 25 μA) to increase the UVP pin voltage and to, by this means, generate a programmable hysteresis.

The hysteresis additional amount is given by the following equation:

$$H_{uvp} = \left((R_{uvp1}//R_{uvp2}) + R_{uvp3}\right) \cdot I_{uvp} \qquad \text{(eq. 28)}$$

In our case, R_{uvp3} is 10 kΩ, hence:

$$H_{uvp} = (10\ k//15\ k) + 10\ k) \cdot 25\ \mu = 400\ mV \qquad \text{(eq. 29)}$$

Therefore, the UVP threshold is:

- 2.06 V typically, when the part is off as a fault is detected (the "V_{uvp}" voltage of Figure 6 must exceed 2.06 V to enable the part)
- 1.6 V when no fault is detected, as a consequence of the 400 mV programmed hysteresis that is added to the 60 mV permanent inbuilt hysteresis. The "V_{uvp}" voltage of Figure 6 must go below 1.6 V to trigger the UVP protection.

Step 3 − Regulation Loop

A NCP4331 driven post−regulator is different from a traditional buck regulator in that its input voltage is pulsed. However, on the regulation point of view, it can be considered as a traditional voltage mode buck converter. Hence, we recommend the implementation of a type 3 compensation network.

The transfer function of the buck post regulator is:

$$\frac{V_{out}}{EA_{out}} = d(EA_{out}) \cdot V_{in} \cdot \frac{1 + (s \cdot r_c \cdot C_{bulk})}{1 + \left(s \cdot \left(\frac{L}{R} + ((r_L + r_c) \cdot C_{bulk})\right)\right) + (s^2 \cdot L \cdot C_{bulk})} \qquad \text{(eq. 30)}$$

Where:

- V_{in} is the amplitude of the pulsed input voltage
- G_0 is the gain of the PWM circuitry that sets the duty− ratio as a function of the error amplifier output EA_{out}
- r_L is the coil series resistor
- r_c is the series resistor of the output capacitor
- R is the load equivalent resistance

The (large signal) analysis of the NCP4331 operation would show that:

$$d = 1 - \frac{C_{RAMP} \cdot (V_{PWM} - EA_{out}) \cdot f_{SW}}{I_{RAMP}} \qquad \text{(eq. 31)}$$

Where:

- d is the duty ratio
- f_{sw} is the switching frequency
- C_{RAMP} is the timing capacitor connected to pin8
- I_{RAMP} is the C_{ramp} charge current
- V_{PWM} is the internal PWM threshold (3 V typically).

Hence, the modulator (small signal) gain is :

$$d(EA_{out}) = \frac{C_{RAMP} \cdot f_{SW}}{I_{RAMP}} \qquad \text{(eq. 32)}$$

And after we note that the term $\left(\frac{R}{r_L + R}\right)$ of Equation 31 can be neglected since (r_L) is very small compared to R even at full load (Note 5) $\left(R = \frac{3.3\ V}{20\ A} = 165\ m\Omega\right)$

5. This term will be neglected in the rest of the document for the sake of simplicity.

$$\frac{V_{out}}{EA_{out}} = G_0 \cdot \frac{1 + (s \cdot r_c \cdot C_{bulk})}{1 + \left(s \cdot \left(\frac{L}{R} + ((r_L + r_c) \cdot C_{bulk})\right)\right) + (s^2 \cdot L \cdot C_{bulk})} \quad \text{where:} \quad G_0 = \frac{C_{RAMP} \cdot f_{SW} \cdot V_{in}}{I_{RAMP}} \quad \text{(eq. 33)}$$

Finally, the Bode plot (dB) of the power stage gain can be represented as follows where (−1) and (−2) indicate respectively, a −20 and a −40 dB per decade attenuation:

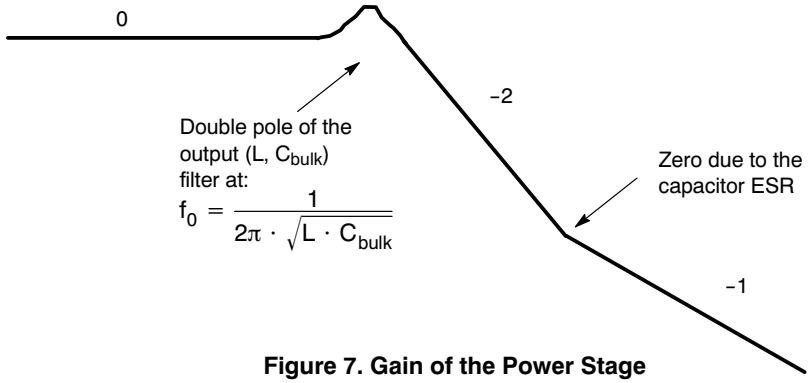

Figure 7. Gain of the Power Stage

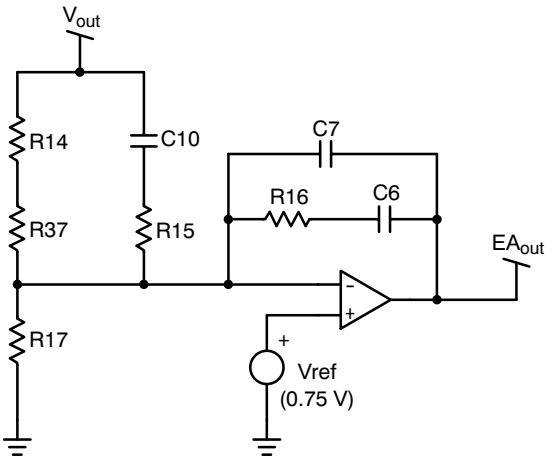

Figure 8. Type 3 Compensation (Labels Correspond to those of the Application Schematic)

The transfer function of the compensator portrayed by Figure 8, is:

$$\frac{EA_{out}}{V_{out}} = \frac{\left(1 + s \cdot (R_{14} + R_{37} + R_{15}) \cdot C_{10}\right) \cdot (1 + s \cdot R_{16} \cdot C_6)}{s \cdot (R_{14} + R_{37}) \cdot (C_6 + C_7)(1 + s \cdot R_{15} \cdot C_{10}) \cdot \left(1 + s \cdot R_{16} \cdot \frac{C_6 \cdot C_7}{C_6 + C_7}\right)} \quad \text{(eq. 34)}$$

Generally, $C_7 << C_6$, hence the precedent equation simplifies as follows:

$$\frac{EA_{out}}{V_{out}} = \frac{\left(1 + \frac{s}{2\pi \cdot f_{z1}}\right) \cdot \left(1 + \frac{s}{2\pi \cdot f_{z2}}\right)}{\frac{s}{2\pi \cdot f_{p0}} \cdot \left(1 + \frac{s}{2\pi \cdot f_{p1}}\right) \cdot \left(1 + \frac{s}{2\pi \cdot f_{p2}}\right)} \quad \text{(eq. 35)}$$

Where: $f_{p0} = \frac{1}{2\pi \cdot (R_{14} + R_{37}) \cdot C_6}$ (pole at the origin)

$f_{p1} = \frac{1}{2\pi \cdot R_{15} \cdot C_{10}}$

$f_{p2} = \frac{1}{2\pi \cdot R_{16} \cdot C_7}$

$f_{z1} = \frac{1}{2\pi \cdot (R_{14} + R_{37} + R_{15}) \cdot C_{10}}$

$f_{z2} = \frac{1}{2\pi \cdot R_{16} \cdot C_6}$

The zeroes being placed at lower frequencies compared to the poles, the following characteristic is obtained:

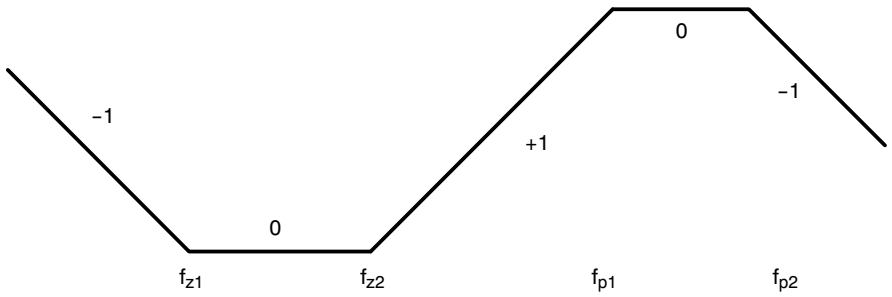

Figure 9. Gain of the Compensator

We need then to place these poles and zeroes so that the open loop gain crosses zero at the crossover frequency f_c with a (−1) slope and the wished phase margin.

Several methods are possible like the k factor of Dean Venable.

Here, we propose to compensate our post−regulator by systematically forcing a (−1) slope for the open loop gain up to the crossover frequency. The advantage of the method is that it does not require the measurement nor the computation of the open loop gain at the crossover frequency.

It can be done as follows:

a. Select the crossover frequency f_c. It is generally admitted that it should be less than one fifth of the switching frequency and at least, three times above the resonant frequency. In our case (f_c = 10 kHz) is chosen (Note 6).

b. Position coincident zeroes at the resonant frequency to cancel the double pole: ($f_{z1} = f_{z2} = f_0$).

c. Place f_{p2} at half the switching frequency:

$$\left(f_{p2} = \frac{f_{SW}}{2}\right)$$

This pole filters the high frequency noise and forces the gain to further roll−off.

d. Use f_{p1} to cancel the zero resulting from the bulk capacitor ESR:

$$\left(f_{p1} = \frac{1}{2\pi \cdot r_c \cdot C_{bulk}}\right)$$

If the ESR zero is at high frequency, you can clamp f_{p1} at half the switching frequency

$$\left(f_{p1} = f_{p2} = \frac{f_{SW}}{2}\right)$$

e. The poles and zeroes of the power stage are cancelled by the zeroes and poles of the compensator so that the pole at the origin f_{p0} forces a (−1) slope. Hence, all the other poles and zeroes being “neutralized”, the pole at the origin is to set as the function of the static gain G_0 so that the open loop gain to be zero at the crossover frequency:

$$\left(f_{p0} = f_c \cdot 10^{-\frac{G_0}{20}}\right)$$

G_0 being expressed in dB.

In our application:

a. (f_c = 10 kHz)

b. The resonant frequency is:

$$f_0 = \frac{1}{2\pi\sqrt{L \cdot C_{bulk}}} = \frac{1}{2\pi\sqrt{5\,\mu \cdot 2.4\,m}} \cong 1.4\ kHz$$

$$f_{z1} = \frac{1}{2\pi \cdot (R_{14} + R_{37} + R_{15}) \cdot C_{10}} = 1.4\ kHz$$

$$f_{z2} = \frac{1}{2\pi \cdot R_{16} \cdot C_6} = 1.4\ kHz$$

c. One pole (f_{p2}) can be selected above the crossover frequency to filter the switching ripple and force the gain to further roll−off. The switching frequency being 70 kHz, let’s choose:

$$f_{p2} = \frac{1}{2\pi \cdot R_{16} \cdot C_7} = 35\ kHz$$

d. The ESR being in the range of 13 mΩ, the “ESR zero” frequency is 5.1 kHz and:

$$f_{p1} = \frac{1}{2\pi \cdot R_{15} \cdot C_{10}} = 5.1\ kHz$$

e. The static gain of the power stage is:

$$G_0 = 20 \cdot \log\left(\frac{C_{ramp} \cdot f_{SW} \cdot V_{in}}{I_{ramp}}\right) = 22.4\ dB$$

Select the pole at the origin so that based on the above computed static gain, the wished crossover frequency is obtained:

$$f_{p0} = f_c \cdot 10^{-\frac{G_{f_c}}{20}} = 10\ k \cdot 10^{-\frac{22.4}{20}} \cong 760\ Hz$$

6. It is generally admitted that the crossover frequency of the post−regulator should be well separated from that of the main converter. This is to minimize the risk of beat frequency between the two loops.

From the above equations, we can deduce:

$$\frac{f_{z1}}{f_{p1}} = \frac{R15}{33\ k + 0.91\ k + R15} = \frac{1.4}{5.1} \Rightarrow R15 = 12.8\ k\Omega \qquad (R_{15} = 12\ k\Omega) \text{ can be used.} \qquad \text{(eq. 36)}$$

$$C_{10} = \frac{1}{2\pi \cdot 5.1\ k \cdot 12\ k} = 2.6\ nF \qquad (C_{10} = 2.7\ nF) \text{ can be used.} \qquad \text{(eq. 37)}$$

$$C_6 = \frac{1}{2\pi \cdot 760 \cdot 33.91\ k} \cong 6.2\ nF \qquad (C_6 = 6.8\ nF) \text{ can be used.} \qquad \text{(eq. 38)}$$

$$C_7 = \frac{1}{2\pi \cdot 35\ k \cdot 33.91\ k} = 134\ pF \qquad (C_7 = 220\ pF) \text{ can be used.} \qquad \text{(eq. 39)}$$

$$R_{16} = \frac{1}{2\pi \cdot 1.4\ k \cdot 6.8\ n} = 16.7\ k\Omega \qquad (R_{16} = 18\ k\Omega) \text{ can be used.} \qquad \text{(eq. 40)}$$

Please note using this method, the phase margin asymptotically tends towards 90°. In other words, the system must be extremely stable but might be a bit slow (long recovery first order response). It can be shown that we can generally consider 75° as an excellent trade off between speed and voltage bounce.

The phase margin is the difference between 360°C, i.e., the lag limit not to exceed, and the phase at the crossover frequency. Taking into account:

- the 180° phase reversal due to the error amplifier,
- the 90° phase shift resulting from the pole of the origin
- the zeroes of the open−loop transfer function that bring a phase lead depending of their position with respect to the crossover frequency
- the poles of the open−loop transfer function that bring a phase lag depending of their position with respect to the crossover frequency

The following equation returns the phase margin: $\Phi_m = 360° - 180° - 90° + \sum_i \arctan\left(\frac{f_c}{f_{z_i}}\right) - \sum_i \arctan\left(\frac{f_c}{f_{p_i}}\right)$ (eq. 41)

Where (f_{z1}) are the the zeroes of the open loop transfer function and (f_{p1}) the poles (apart from the pole at the origin). Hence, the phase margin exhibited by our loop is given by:

$$\Phi_m = 90° + \arctan\left(\frac{f_c}{f_{z1}}\right) + \arctan\left(\frac{f_c}{f_{z2}}\right) + \arctan\left(\frac{f_c}{f_{z_{ESR}}}\right) - \left(2 \cdot \arctan\left(\frac{f_c}{f_0}\right)\right) - \arctan\left(\frac{f_c}{f_{p1}}\right) - \arctan\left(\frac{f_c}{f_{p2}}\right) \qquad \text{(eq. 42)}$$

In our case:

- $f_{z1} = f_{z2} = f_0$
- $f_{p1} = f_{ZESR}$

Hence, the precedent equation simplifies as follows:

$$\Phi_m \cong 90° - \arctan\left(\frac{f_c}{f_{p2}}\right) \qquad \text{(eq. 43)}$$

In our first choice, we have selected (f_{p2} = 35 kHz), hence:

$$\Phi_m \cong 90° - \arctan\left(\frac{10\ k}{35\ k}\right) = 74° \qquad \text{(eq. 44)}$$

If a different phase margin is wished, the distance between f_0 and f_{p2} can be changed.

For instance, if you target 45°, choose f_{p2} so that:

$$90° - \arctan\left(\frac{f_c}{f_{p2}}\right) = 45° \qquad \text{(eq. 45)}$$

$$\text{Then: } f_{p2} = \frac{f_c}{\tan(45°)} = f_c \qquad \text{(eq. 46)}$$

To do so, in our design, C_7 has to be increased to 470 pF.

Step 4 – Current Limitation

The NCP4331 embeds a second operational amplifier (OPAMP2) to perform a Constant Current Constant Voltage control (CCCV). In other words, if the output current exceeds a preset threshold, this OPAMP2 reduces the output of the main error amplifier to limit the duty−ratio. Ultimately, the current excess is cancelled.

The output of the two operational amplifiers can be directly connected as shown by Figure 10. This is because:

- The two operational amplifiers are similarly built. They can be viewed as “SINK only operational amplifiers” that are biased by an internal current source (I_{bias1} for OPAMP1 and I_{bias2} for OPAMP2 – see Figure 10). They adjust their output level by absorbing part or more than this current in response to the error they amplify.
- When the two output are connected (pin1 and pin 5), the current sources add and become the biasing current for the one OPAMP that needs to set the lowest level (OPAMP1 if the inductor current is within the permissible range, OPAMP2 otherwise). This is possible since both of them feature a sinking capability that is greatly sufficient to absorb the sum of the two current sources ($I_{bias1} + I_{bias2}$).

Hence, the two operational amplifiers can then be coupled directly without the need for diodes.

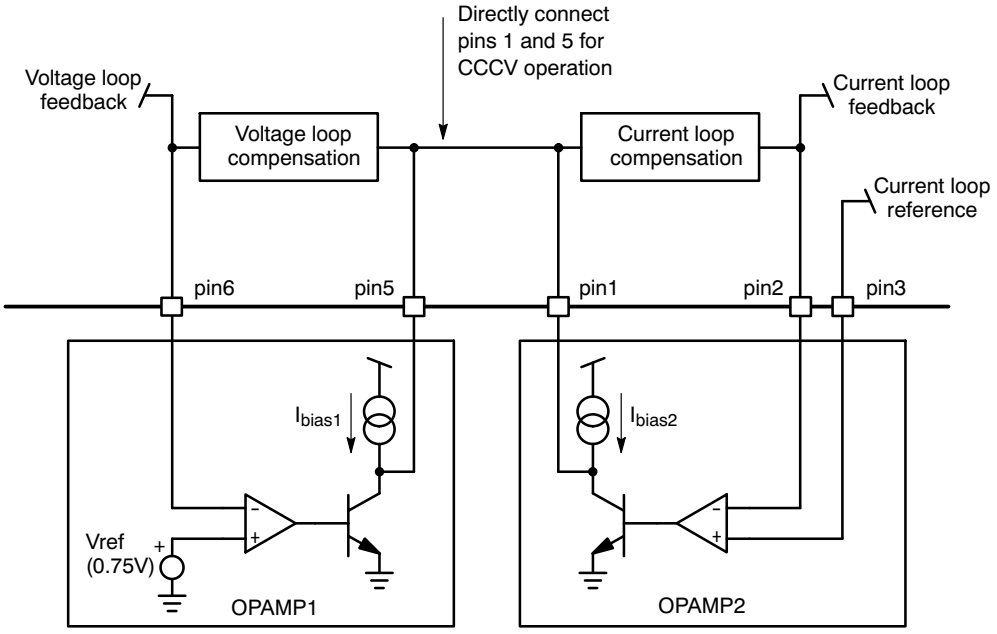

Figure 10. Implementation for CCCV

Remarks:

- If you don’t need OPAMP2, simply ground pins 1 to 3.
- If wished, OPAMP2 can be used for other purposes than CCCV, like, for instance, for an improved V_{out} tracking of V_{out1} (see Figure 26 of the data sheet) or for over−voltage protection (see Figure 26 of the data sheet).
- Other usages can be considered as a negative current detection in which pin1 would drive the UVP pin...

Sensing the Current

Now, unlike the output voltage, the output current is not easy to sense because a) the insertion of a current sense resistor is not an efficiency way (too high ohmic losses) and b) measuring a dc current by a magnetic means is not an easy task...

We would then recommend to sense the coil current (its average value is I_{out}) by utilizing the inductor series resistor. Figure 11 portrays how it can be done.

A (R, C) network is placed across the inductor and the resulting capacitor voltage V_C is used as the feedback information. Some algebra manipulations would show that V_C is linked to the instantaneous coil current I_L, as follows:

$$\frac{V_c}{r_L \cdot I_L} = \frac{1 + \left(s \cdot \frac{L}{r_L}\right)}{1 + \left(s \cdot \frac{R_{s1,1} \cdot R_{s1,2} \cdot C_s}{R_{s1,1} + R_{s1,2}}\right)}$$

A dc analysis of the voltage applied to pin2 (inverting input of the second operational amplifier OPAMP2 that is embedded in the NCP4331) is:

$$V_{pin2} = k_1 \cdot \left(V_{out} + (r_L \cdot I_L)\right) \qquad \text{(eq. 47)}$$

$$\text{where } k_1 = \frac{R_{s2}}{R_{s1,1} + R_{s1,2} + R_{s2}}$$

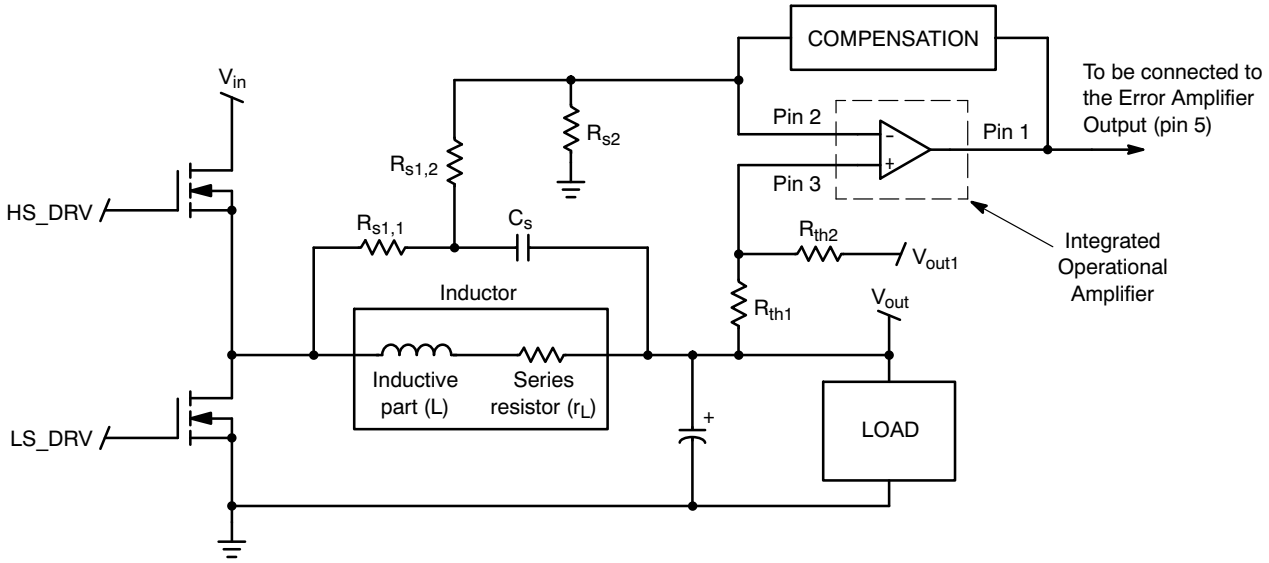

Figure 11. Circuitry for Sensing the Inductor Current

On the other hand, the non−inverting input of OPAMP2 receives:

$$V_{pin3} = k_2 \cdot \left(V_{out} + \left(\frac{R_{th1}}{R_{th2}} \cdot V_{out1} \right) \right) \text{ where } k_2 = \frac{R_{th2}}{R_{th1} + R_{th2}} \quad \text{(eq. 48)}$$

Finally, OPAMP2 amplifies the following error:

$$V_{pin3} - V_{pin2} = \left((k_2 - k_1) \cdot V_{out} \right) + \left(k_2 \cdot \frac{R_{th1} \cdot V_{out1}}{R_{th2}} \right) - (k_1 \cdot r_L \cdot I_L) \quad \text{(eq. 49)}$$

We can choose ($k_1 = k_2$) by simply selecting:

$R_{th1} = R_{s1,1} + R_{s1,2}$

$R_{th2} = R_{s2}$

In this condition ($k_1 = k_2$), the precedent equation dramatically simplifies as follows:

$$V_{pin3} - V_{pin2} = k_1 \cdot \left(\frac{R_{th1} \cdot V_{out1}}{R_{th2}} - (r_L \cdot I_L) \right)$$

Therefore, the voltage across the inductor series resistor is compared to

$$\left(\frac{R_{th1} \cdot V_{out1}}{R_{th2}} \right)$$

and we can deduce the following current limitation:

$$I_{L,max} = \frac{\frac{R_{th1} \cdot V_{out1}}{R_{th2}}}{r_L} \quad \text{(eq. 50)}$$

In our application, ($R_{s1,1} + R_{s1,2} = R_{th1} = 2.2\ k\Omega$) and ($R_{s2} = R_{th2} = 100\ k\Omega$). Hence, since V_{out1} is 5 V and r_L is 4.7 mΩ maximum, the minimal current limit is set to:

$$I_{L,max} \geq \frac{2.2\ k}{100\ k} \cdot \frac{5}{4.7\ m} \cong 23\ A \quad \text{(eq. 51)}$$

($R_{s1,1}$ = 1.2 kΩ), ($R_{s1,2}$ = 1.0 kΩ) and (C_s = 1 μF) were implemented to sense the coil current (R_{33}, R_3 and C_2 of the application schematic).

Selecting ($k_1 = k_2$) has another merit. As shown above, the pins 2 and 3 voltages are referenced to the output voltage. Choosing ($k_1 = k_2$) makes equal the portion of V_{out} that is applied to the 2 pins. Hence, the compensation network can be represented by the simplified Figure 12.

Remark:

If not specified by the vendor, the indictor series resitor can be measured by forcing a dc current (preferably the full load current − ($I_{L(dc)}$ = 20 A) in our case) within the coil and, once the steady state temperature has been reached, by measuring the inductor voltage:

$$r_L = \frac{V_L}{I_{L(dc)}}$$

Compensating the Current Loop

If we consider a resistive load R, the output current is

$$\left(\frac{V_{out}}{R} \right)$$

The transfer function linking V_{out} to the error amplifier output EA_{out} has been already derived in the voltage loop section. From it, we can easily deduce the transfer function

$$\left(\frac{I_{out}}{EA_{out}} \right):$$

$$\frac{I_{out}}{EA_{out}} = \frac{G_0}{R} \cdot \frac{1 + (s \cdot r_c \cdot C_{bulk})}{1 + \left(s \cdot \left(\frac{L}{R} + \left((r_L + r_c) \cdot C_{bulk}\right)\right)\right) + (s^2 \cdot L \cdot C_{bulk})} \quad \text{where : } G_0 = \frac{C_{RAMP} \cdot f_{SW} \cdot V_{in}}{I_{RAMP}} \qquad \text{(eq. 52)}$$

where R is the (equivalent) load resistor.

Now, the coil current feeds the output capacitor and the load. In case of a resistive load, we can write the general relation linking I_L and I_{out} by considering the coil current sharing between the two parallel loads consisting of the capacitor and the output resistor:

$$\frac{I_L}{I_{out}} = \frac{1 + \left(s \cdot (r_c + R) \cdot C_{bulk}\right)}{1 + (s \cdot r_c \cdot C_{bulk})} \qquad \text{(eq. 53)}$$

Finally, substitution of Equation 53 into Equation 52 leads to the following transfer function:

$$\frac{r_L \cdot I_L}{EA_{out}} = G_{c_0} \cdot \frac{\left(1 + \frac{s}{2\pi \cdot f''_z}\right)}{1 + \left(s \cdot \left(\frac{L}{R} + \left((r_L + r_c) \cdot C_{bulk}\right)\right)\right) + (s^2 \cdot L \cdot C_{bulk})} \qquad \text{(eq. 54)}$$

$$\text{where : } G_0 = \frac{r_L}{R} \cdot \frac{C_{RAMP} \cdot f_{SW} \cdot V_{in}}{I_{RAMP}} \qquad \text{and : } f''_z = \frac{1}{2\pi \cdot (r_c + R) \cdot C_{bulk}}$$

Like for the voltage loop, we have to compensate a system that has the characteristic of a CCM voltage mode boost converter. Therefore, again, a type 3 compensation is recommended.

The procedure proposed for the voltage loop can be re−used.

However, we can note that the equation shows the presence of a low frequency zero. Instead of cancelling it, we can use it to partly compensate the resonant double pole and a type 2 compensation becomes sufficient (see Figure 12).

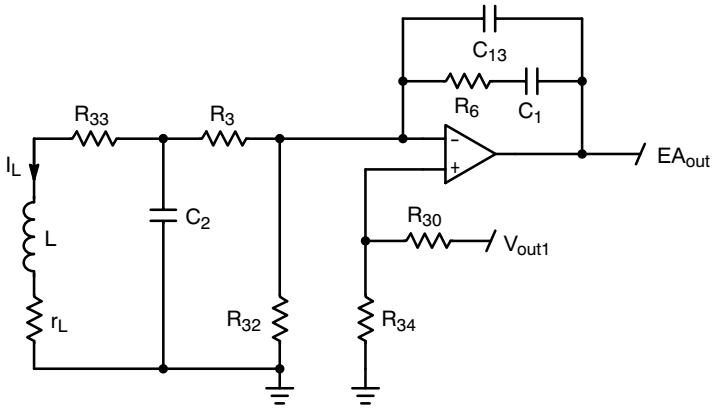

Figure 12. Current Loop Compensation
(labels correspond to those of the application schematic)

If as indicated in the “sensing the current” section, we need to have ($R_{s1,1} + R_{s1,2} = R_{th1}$) and ($R_{s2} = R_{th2}$), or using the labels of Figure 12: ($R_3 + R_{33} = R_{30}$) and ($R_{32} = R_{34}$). In these conditions, the transfer function of the compensator is:

$$\frac{EA_{out}}{r_L \cdot I_L} = \frac{1 + \left(s \cdot \frac{L}{r_L}\right)}{1 + \left(s \cdot \frac{R_{33} \cdot R_3 \cdot C_2}{R_{33} + R_3}\right)} \cdot \frac{(1 + s \cdot R_6 \cdot C_1)}{s \cdot (R_3 + R_{33}) \cdot (C_1 + C_{13}) \cdot \left(1 + s \cdot R_6 \cdot \frac{C_1 \cdot C_{13}}{C_1 + C_{13}}\right)} \qquad \text{(eq. 55)}$$

This equation significantly simplifies $\left(\text{if } \frac{R_{33} \cdot R_3 \cdot C_2}{R_{33} + R_3} = \frac{L}{r_L}\right)$

(in this case, the voltage across the C_2 capacitor is simply ($r_L \cdot I_L$)). As in addition, $C_{13} << C_1$, the precedent equation becomes:

$$\frac{EA_{out}}{r_L \cdot I_L} = \frac{\left(1 + \frac{s}{2\pi \cdot f'_{z1}}\right)}{\frac{s}{2\pi \cdot f'_{p0}} \cdot \left(1 + \frac{s}{2\pi \cdot f'_{p1}}\right)} \qquad \text{(eq. 56)}$$

Where:

$$f'_{p0} = \frac{1}{2\pi \cdot (R_3 + R_{33}) \cdot C_1} \quad \text{(pole at the origin)}$$

$$f'_{p1} = \frac{1}{2\pi \cdot R_6 \cdot C_{13}}$$

$$f'_{z1} = \frac{1}{2\pi \cdot R_6 \cdot C_1}$$

Remark:

You may not be comfortable in selecting R_3, R_{33} and C_2 so that

$$\left(\frac{R_{33} \cdot R_3 \cdot C_2}{R_{33} + R_3} = \frac{L}{r_L}\right),$$

in particular if this would lead to an "inconvenient" C_s capacitor. In this case, choose the C_s capacitor you like, possibly close to the wished value. Simply, you must take into account that the pole

$$f_{p_s} = \left(\frac{1}{2\pi \cdot \frac{R_{33} \cdot R_3}{R_{33} + R_3} \cdot C_2}\right)$$

does not exactly cancel the zero produced by L and r_L at

$$f_{z_{Lr}} = \left(\frac{1}{2\pi \cdot \frac{L}{r_L}}\right)$$

by estimating the impact it will have on the gain:

(eq. 57)

$$\Delta G_{S_{dB}} = 20 \cdot \log\frac{f_{P_s}}{f_{Z_{Lr}}} = 20 \cdot \log\left(\frac{(R_{33} + R_3) \cdot L}{R_{33} \cdot R_3 \cdot C_S \cdot r_L}\right)$$

where ΔG_{SdB} the possible gain increase due to the current sense network.

In our case:

(eq. 58)

$$\Delta G_{S_{dB}} = 20 \cdot \log\left(\frac{(1.2\text{ k} + 1\text{ k}) \cdot 5\ \mu}{1.2\text{ k} \cdot 1\text{ k} \cdot 1\ \mu \cdot 4\text{ m}}\right) \cong 7.2\text{ dB}$$

Again, one can compensate our post−regulator by systematically forcing a (−1) slope for the open loop gain up to the crossover frequency. It can be done as follows:

a. Select the crossover frequency f_c. Let's choose the same crossover frequency as the one selected for the voltage loop: (f_c = 10 kHz)

b. Let's position the compensator zero at the resonant frequency

$$\left(f'_{z1} = \frac{1}{2\pi \cdot R_6 \cdot C_1} = f_0\right)$$

c. Place f'_{p1} at half the switching frequency

$$\left(f'_{p1} = \frac{f_{SW}}{2}\right)$$

This pole filters the high frequency noise.

d. Let's calculate the zero brought by the transfer function

$$\left(\frac{r_L \cdot I_L}{EA_{out}}\right)$$

at full load (R = 165 mΩ):

$$f''_z = \frac{1}{2\pi \cdot (r_c + R) \cdot C_{bulk}} = \frac{1}{2\pi \cdot (13\text{ m} + 165\text{ m}) \cdot 2.4\text{ m}} \cong 373\text{ Hz}$$

e. The f'_{p0} frequency must be set so that the gain crosses 0 at (f_c = 10 kHz). In other words, we have to compute G_{fc}, i.e., the gain of the system @ ($f = f_c$) and @ full load (maximum current). As done when computing (ΔG_{SdB}) (see Equations 1−13), the G_{fc} calculation must take into account the (f″z) position that has an attenuation effect if placed above the resonant frequency or an amplification effect if placed below:

$$\left(\Delta G_{z''dB} = 20 \cdot \log\frac{f_0}{f''_z}\right) \quad \text{(eq. 59)}$$

Then, we need to position the pole at the origin to force the open loop gain to be zero at the crossover frequency:

$$\left(f_{p_0} = f_c \cdot 10^{\frac{G_{fc}}{20}}\right)$$

where: $G_{f_c} = 20 \cdot \log G_{C_0} + \Delta G_{S_{dB}} + \Delta G_{z''_{dB}}$ (eq. 60)

where G_{c0} is the static gain defined by Equation 54

ΔG_{Sdb} and $\Delta G_{Z''db}$ are the gain increase resulting from the non pole−zero neutralization, defined by Equations 57 and 63 respectively.

In our application:

a. (f_c = 10 kHz)

b. The resonant frequency is:

$$f_0 = \frac{1}{2\pi\sqrt{L \cdot C_{bulk}}} = \frac{1}{2\pi\sqrt{5\ \mu \cdot 2.4\text{ m}}} \cong 1.4\text{ kHz}$$

$$f'_{z1} = f_0 \Rightarrow \frac{1}{2\pi \cdot R_6 \cdot C_1} = 1.4\text{ kHz}$$

c. The pole (f'_{p2}) should be selected to filter the switching ripple. The switching frequency being 70 kHz, let's choose:

$$f'_{p2} = \frac{1}{2\pi \cdot R_6 \cdot C_{13}} = 35\text{ kHz}$$

d. The gain @ ($f = f_c$) is:

$$(G_{fc})_{dB} = 20 \cdot \log G_{C_0} + \Delta G_{S_{dB}} + \Delta G_{z''_{dB}} = 20 \cdot \log\left(\frac{4\text{ m} \cdot 470\text{ p} \cdot 70\text{ k} \cdot 20}{165\text{ m} \cdot 50\ \mu}\right) + 20 \cdot \log\left(\frac{1.4\text{ k}}{373}\right) + 7.2 \cong 8.8\text{ dB}$$

e. Select the pole at the origin so that based on the above computed static gain, the wished crossover frequency is obtained:

$$f'_{p0} = f_c \cdot 10^{-\frac{G_{fc}}{20}} = 10\,k \cdot 10^{-\frac{1.6}{20}} \cong 3.6\,kHz$$

From the above equations, we can deduce:

$$f'_{p0} = \frac{1}{2\pi \cdot (R_3 + R_{33}) \cdot C_1} = 3.6\,kHz \Rightarrow C_1 = \frac{1}{2\pi \cdot 2.2\,k \cdot 3.6\,k} \cong 19.9\,nF \quad (C_1 = 22\,nF) \text{ can be used} \quad \text{(eq. 61)}$$

$$f'_{z1} = \frac{1}{2\pi \cdot R_6 \cdot C_1} = 1.4\,kHz \Rightarrow R_6 \cong 5.17\,k\Omega \quad (R_6 = 5.1\,k\Omega) \text{ can be used} \quad \text{(eq. 62)}$$

$$f'_{p2} = \frac{1}{2\pi \cdot R_6 \cdot C_{13}} = 35\,kHz \Rightarrow C_{13} \cong 892\,pF \quad (C_{13} = 820\,pF) \text{ can be used} \quad \text{(eq. 63)}$$

Again, one must note that with this method, the phase margin asymptotically tends towards 90°. If a lower phase margin is wished to speed−*up the dynamic response, we can proceed as done with the voltage loop, i.e., play with the high frequency pole to adjust the wished phase margin:

$$\Phi_m = 90^o - \arctan\left(\frac{f_c}{f'_{p2}}\right) = 90^o - \arctan(2\pi \cdot R_6 \cdot C_{13} \cdot f_c) \quad \text{(eq. 64)}$$

Our design returns a 75° phase margin that is generally considered as a good one.

Solution with a Specific Current Sense Resistor

If you cannot rely on the resistor of the coil to measure the current, a current sense resistor can be inserted as shown in the following figure. It is important that the resistance is very low not to degrade the efficiency.

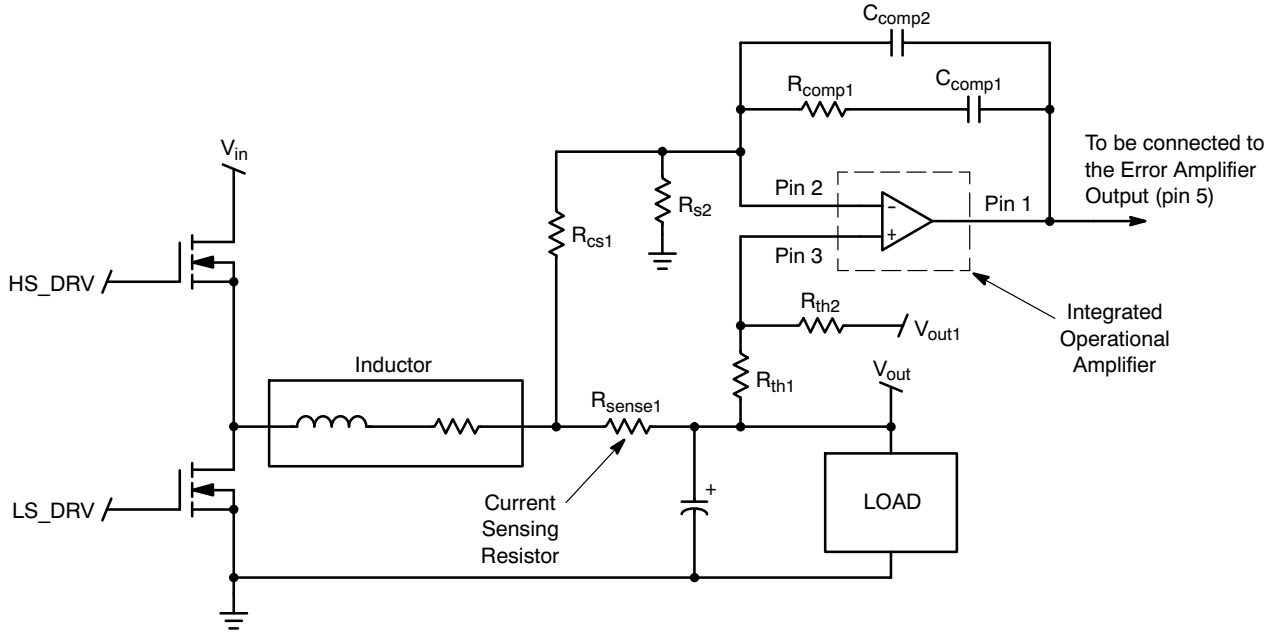

Figure 13. Circuitry where a Specific Resistor Senses the Current

In this configuration, the previous considerations can be re−used so that finally, the system can be summarized as follows:

Over−Current Threshold:

We recommend to choose: ($R_{cs1} = R_{th1}$) and ($R_{cs2} = R_{th2}$) so that:

$$I_{L,max} = \frac{\frac{R_{th1} \cdot V_{out1}}{R_{th2}}}{R_{sense1}}$$

For instance, we can select:

- $R_{cs1} = R_{th1} = 2.2\,k\Omega$
- $R_{cs2} = R_{th2} = 100\,k\Omega$
- $R_{sense1} = 4\,m\Omega$

With this selection, if V_{out1} is 5 V:

$$I_{L,max} = \frac{\frac{2.2\,k \cdot 5}{100\,k}}{4\,m} = 27.5\,A$$

Power Stage Transfer Function:

$$\frac{R_{sense1} \cdot I_L}{EA_{out}} = \frac{R_{sense1} \cdot G_0}{R} \cdot \frac{\left(1 + \frac{s}{2\pi \cdot f''_z}\right)}{1 + \left(s \cdot \left(\frac{L}{R} + \left((r_L + r_c) \cdot C_{bulk}\right)\right)\right) + (s^2 \cdot L \cdot C_{bulk})} \quad \text{(eq. 65)}$$

where: $G_0 = \frac{C_{RAMP} \cdot f_{SW} \cdot V_{in}}{I_{RAMP}}$ and $f''_z = \frac{1}{2\pi \cdot (r_c + R) \cdot C_{bulk}}$

Compensator Transfer Function:

$$\frac{EA_{out}}{R_{sense1} \cdot I_L} = \frac{\left(1 + \frac{s}{2\pi \cdot f'''_{z1}}\right)}{\frac{s}{2\pi \cdot f'''_{p0}} \cdot \left(1 + \frac{s}{2\pi \cdot f'''_{p1}}\right)} \quad \text{(eq. 66)}$$

Where:

$$f'''_{p0} = \frac{1}{2\pi \cdot R_{cs1} \cdot C_{comp1}} \quad \text{(pole at the origin)}$$

$$f'''_{p1} = \frac{1}{2\pi \cdot R_{comp1} \cdot C_{comp2}}$$

$$f'''_{z1} = \frac{1}{2\pi \cdot R_{comp1} \cdot C_{comp1}}$$

C_{comp2} being considered as very small compared to C_{comp1}.

Closing the Loop:

If we use the previous method:

a. (f_c = 10 kHz)

b. The resonant frequency is:

$$f_0 = \frac{1}{2\pi\sqrt{L \cdot C_{bulk}}} = \frac{1}{2\pi\sqrt{5\ \mu \cdot 2.4\ m}} \cong 1.4\ kHz$$

$$f'_{z1} = f_0 \Rightarrow \frac{1}{2\pi \cdot R_6 \cdot C_1} = 1.4\ kHz$$

c. The pole (f'''_{p2}) should be selected to filter the switching ripple. The switching frequency being 70 kHz, let's choose:

$$f'''_{p2} = \frac{1}{2\pi \cdot R_{comp1} \cdot C_{comp2}} = 35\ kHz$$

d. The gain @ ($f = f_c$) is:

$$(G_{fc})_{dB} = 20 \cdot \log\left(\frac{R_{sense1} \cdot C_{ramp} \cdot f_{SW} \cdot V_{in}}{R \cdot I_{ramp}} \cdot \frac{f_0}{f''_z}\right) = 20 \cdot \log\left(\frac{4\ m \cdot 470\ p \cdot 70\ k \cdot 20}{165\ m \cdot 50\ \mu} \cdot \frac{1.4\ k}{373}\right) \cong 1.6\ dB$$

e. Select the pole at the origin so that based on the above computed static gain, the wished crossover frequency is obtained:

$$f'''_{p0} = f_c \cdot 10^{-\frac{G_{fc}}{20}} = 10\ k \cdot 10^{\frac{1.6}{20}} \cong 8.3\ kHz$$

From the above equations, we can deduce:

$$f'''_{p0} = \frac{1}{2\pi \cdot R_{cs1} \cdot C_{comp1}} = 8.3\ kHz \Rightarrow C_{comp1} = \frac{1}{2\pi \cdot 2.2\ k \cdot 8.3\ k} \cong 8.7\ nF \quad \text{(eq. 67)}$$

$$f'''_{z1} = \frac{1}{2\pi \cdot R_{comp1} \cdot C_{comp1}} = 1.4\ kHz \Rightarrow R_6 \cong 11.4\ k\Omega \quad \text{(eq. 68)}$$

$$f'''_{p2} = \frac{1}{2\pi \cdot R_{comp1} \cdot C_{comp2}} = 35\ kHz \Rightarrow C_{13} \cong 379\ pF \quad \text{(eq. 69)}$$

Again, the phase margin can be adjusted by playing with the high frequency pole, as follows:

$$\Phi_m = 90^o - \arctan\left(\frac{f_c}{f'''_{p2}}\right) = 90^o - \arctan(2\pi \cdot R_{comp1} \cdot C_{comp2} \cdot f_c) \quad \text{(eq. 70)}$$

Our design returns a 74° phase margin that is generally considered as a good one.

Layout Considerations

A NCP4331−driven post−regulator does not require specific precaution but it seems wise to list the following (traditional) recommendations:

- the tracks conducting the coil current should be as short as possible.
- All the power components (MOSFETs, inductor, capacitor) should be placed in one area of the board.
- The NCP4331 together with the resistors and capacitors necessary to control the post−regulator, should be gathered and placed close to the power components area.
- A power ground connected in a star configuration should be used for the power components.
- A second ground connected in a star configuration should be used for the control components.
- The two grounds should be connected by one single track. Optimally, this track should link the power ground directly to GND pin of the NCP4331.
- Avoid that the driver and V_{CC} currents flow through too long loops and in the vicinity of high impedance signals (like the compensation network). Otherwise, they may disturb them. The return path should not be shared with another control signal (should return to ground by a specific track). The return path for the low−side driver should be the track connecting the two grounds.
- If the synchronization voltage is particularly noisy, it can be helpful to slightly filter the SYNC pin. Few tens of picofarads are generally enough with a synchronization network exhibiting about 10 kΩ. Avoid too large capacitors that could excessively delay the synchronization.
- If the pulsed input voltage V_{in} is used to generate the NCP4331 V_{CC} power source, the implementation of Figure 15 is recommended.

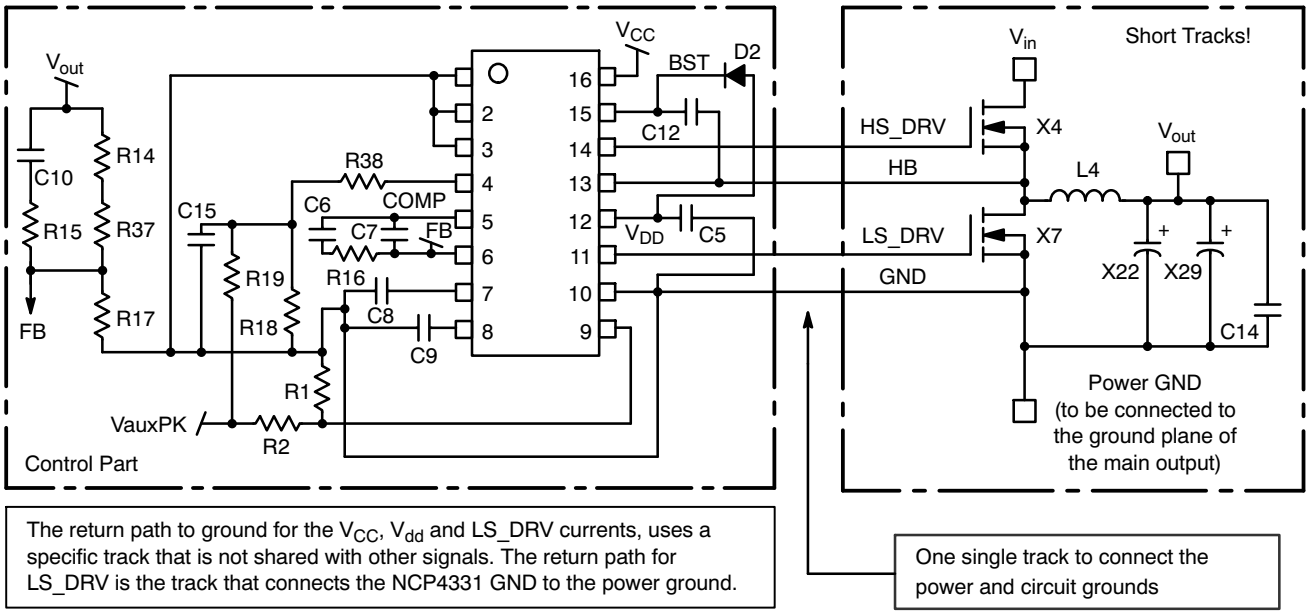

Figure 14. Layout Recommendations

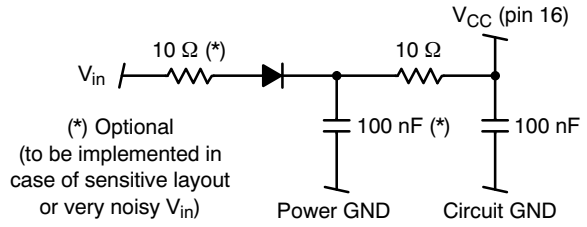

Figure 15. Circuit to Build V_{CC} from V_{in}
(Component Values are Indicative)

Decoupling

A ceramic capacitor is needed between V_{CC} and GND, between V_{dd} and GND and between the "BST" and "HB" pins. The use of 100 nF capacitors is generally a good choice.

As usually, they should be connected as close as possible to the pins. Preferably, the connecting tracks should be specific to the power source that is decoupled and not re−used to convey other signals.

The NCP4331 embeds a regulator that using the V_{CC} voltage (up to 30 V), generates the V_{dd} voltage (7.5 V). The drop across this regulator is as low as 1 V when 20 mA is consumed.

For a more accurate computation of the filtering capacitor to be placed on the V_{CC} pin, we can consider the maximum ripple acceptable across the capacitor during a switching period.

If the circuitry of Figure 15 is used, V_{CC} is charged to the V_{in} peak value (20 V in our application).

Hence, we can tolerate a few volts ripple on V_{CC}. As a rule of the thumb, let's choose ($\Delta V_{CC(max)}$ = 5 V). In this case, assuming that the V_{CC} capacitor discharges for the whole switching period (Note 7):

$$C_{Vcc} \geq \frac{(I_{CC} \cdot T_{SW}) + Q_{total}}{\Delta V_{cc,max}}$$

Where C_{Vcc} is the V_{CC} capacitor, Q_{total} is the total gate charge necessary to drive the high and low−side MOSFETs, I_{cc} is the maximal internal consumption of the circuit.

Practically, I_{cc} is 4 maximum (see data sheet), T_{sw} is 14 μs (70 kHz), Q_{total} is around 200 nC for two MOSFETs charged up to 7.5 V (Note 8), hence:

$$C_{Vcc} \geq \frac{(4\ m \cdot 14\ \mu) + 200\ n}{5} \cong 51\ nF$$

7. This is an extremely simplified and conservative approach since V_{CC} is being charged during the converter on−time (i.e. as long as V_{in} is high)!
8. Q_{total} is over−estimated since the low−side zero voltage switching featured by the NCP4331, significantly reduces the gate charge at turn on.

Summary of the Main Design Equations

This table summarizes the main design equations based on the methodology presented in this application note. Please refer to Figure 16 for the meaning of the computed components.

Steps	Components	Formulae	Comments
Step1 – Coil inductance, bulk capacitor and power MOSFETs	Bulk capacitor	$C_{bulk} \geq \frac{\Delta I_{out}}{2\pi \cdot f_c \cdot 25\% \cdot (\Delta V_{out})_{max}}$ $r_c \leq \frac{75\% \cdot (\Delta V_{out})_{max}}{\Delta I_{out}}$ $(\Delta V_{out})_{max}$ is the permissible deviation under the ΔI_{out} load step	As a rule of the thumb, we assume that if we apply a step load ΔI_{out}, 75% of the resulting deviation is due to the ESR of the capacitor (r_c), 25% being capacitive.
	Inductor	$L \geq \frac{(V_{in} - V_{out}) \cdot V_{out} \cdot \left(r_c + \frac{1}{8 \cdot C_{bulk} \cdot f_{SW}}\right)}{(\Delta V_{out})_{pk-pk} \cdot f_{SW} \cdot V_{in}}$	$(\Delta V_{out})_{pk-pk}$ is the permissable peak to peak output ripple (switching ripple)
	Current ripple across the inductor	$(\Delta I_{out})_{pk-pk} = \frac{(V_{in} - V_{out}) \cdot V_{out}}{L \cdot f_{SW} \cdot V_{in}}$	current peak to peak ripple resulting from the selected inductor (L)
	Output voltage peak to peak ripple	$(\Delta V_{out})_{pk-pk} \leq \left(r_c \cdot (\Delta I_{out})_{pk-pk}\right) + \frac{(\Delta I_{out})_{pk-pk}}{8 \cdot C_{bulk} \cdot f_{SW}}$	
	Resonant frequency	$f_0 = \frac{1}{2\pi \cdot \sqrt{L \cdot C_{bulk}}}$	
	Characteristic impedance	$Z_0 = \sqrt{\frac{L}{C_{bulk}}}$	
	Capacitor ohmic losses	$p_{ESR} = r_c \cdot \frac{(\Delta I_{out})_{pk-pk}^2}{12}$	
	Inductor losses	$P_{r_L} = r_L \cdot \left(I_{out}^2 + \frac{(\Delta I_{out})_{pk-pk}^2}{12}\right)$	r_L is the inductor series resistor
	MOSFETs conduction losses	High−side: $p_{M_{HS}} \cong R_{DS(on)1} \cdot \frac{V_{out}}{V_{in}} \cdot \frac{P_{r_L}}{r_L}$ Low−side: $p_{M_{LS}} \cong R_{DS(on)2} \cdot \frac{(V_{in} - V_{out})}{V_{in}} \cdot \frac{P_{r_L}}{r_L}$	$R_{DS(on)1}$ and $R_{DS(on)2}$ are the on−time resistances of the high and low−side MOSFETs respectively
Step2 – Synchronization, ramp and UVP	Synchronization network	$R_{sync1} \geq \frac{(V_{auxPK})_{max} - 5\ V}{2\ mA}$	
		$R_{sync2} \geq \frac{2.6\ V}{(V_{auxPK})_{min} - 2.6\ V} \cdot R_{sync1}$	
	Ramp capacitor	$C_{RAMP} \geq \frac{26\ \mu}{(f_{SW})_{min}}$	
	Circuitry for Under−Voltage Protection	$(R_{uvp1} // R_{uvp2}) \cdot C_{uvp} \cong \frac{4}{f_{SW}}$	
		$H_{uvp} = \left((R_{uvp1} // R_{uvp2}) + R_{uvp3}\right) \cdot I_{uvp}$	

Steps	Components	Formulae	Comments
Step 3 – Voltage Regulation Loop	Crossover frequency (f_c)	$3 \cdot f_0 \le f_c \le \frac{f_{SW}}{5}$ If f_0 is too high to meet this criterion, increase C_{bulk}.	It is admitted that f_c should be well separated from the crossover frequency of the main converter, to minimize the risk of beating between the two loops
	Gain at $f = f_c$	$G_{f_c} = \frac{C_{RAMP} \cdot f_{SW} \cdot V_{in}}{50\ \mu}$	
	Feedback bottom resistor	$0.5\ k\Omega \le R_{fb2} \le 10\ k\Omega$	R_{fb2} dictates the permanent leakage on V_{out}. Use low values for an improved noise immunity.
	Feedback upper resistor	$R_{fb1} = R_{fb2} \cdot \frac{V_{out} - V_{ref}}{V_{ref}}$	V_{out} is the wished output voltage V_{ref} is the NCP4331 voltage reference (750 mV)
	Compensation elements	$R_3 = \frac{r_c}{Z_0 - r_c} \cdot R_{fb1}$	
		$C_3 = \frac{r_c \cdot C_{bulk}}{R_3}$	
		$C_1 = \frac{G_{f_c}}{2\pi \cdot f_c \cdot R_{fb1}}$	
		$R_1 = \frac{\sqrt{L \cdot C_{bulk}}}{C_1}$	
		$C_2 = \frac{1}{2\pi \cdot f_c \cdot R_1 \cdot \tan(\Phi_{m1})}$	Φ_{m1} is the wished phase margin. It should be between 45° and 90°
Step4 – Current Regulation Loop	Maximum Output Current	$(I_{out})_{max} = \frac{R_{th1} \cdot V_{out1}}{R_{th2} \cdot r_{sense}}$	r_{sense} can be the inductor series resistor (see Figure 11) or a specifically dedicated sensing resistor (see Figure 13).
	Network for current sensing	$R_{s1,1} + R_{s1,2} = R_{th1}$	
		$R_{s2} = R_{th2}$	As a rule of the thumb, 100 kΩ can be used
		$C_s = \frac{R_{s1,1} + R_{s1,2}}{R_{s1,1} \cdot R_{s1,2}} \cdot \frac{L}{r_L}$	To be connected only if the (r_L) senses the current. If more convenient, you can take a 2 or 3 times lower value. The (ΔG_s) term corrects the discrepancy (Note 9).
		$\Delta G_s = \frac{R_{s11} + R_{s12} \cdot L}{R_{s11} \cdot R_{s12} \cdot C_s \cdot r_L}$	Gain boost due to the ($r_L \cdot I_L$) reconstruction from the inductor voltage
		$\Delta G_{z''} = 2\pi \cdot f_0 \cdot (r_c + R) \cdot C_{bulk} = \frac{(r_c + R)}{Z_0}$	Gain boost produced by the current sense circuitry
	Crossover frequency (f_{c2})	$3 \cdot f_0 \le f_{c2} \le \frac{f_{SW}}{5}$	
	Gain at $f = f_{c2}$	$G_{f_{c2}} = \left(\frac{r_{sense} \cdot C_{RAMP} \cdot f_{SW} \cdot V_{in}}{R \cdot 50\ \mu}\right) \cdot \Delta G_s \cdot \Delta G_{z''}$	Take ($\Delta G_s = 1$) with a specific r_{sense} resistor (Figure 13 configuration)
	Compensation elements	$C_{comp1} = \frac{G_{f_{c2}}}{2\pi \cdot f_{c2} \cdot (R_{s1,1} + R_{s1,2})}$	
		$R_{comp1} = \frac{1}{2\pi \cdot f_0 \cdot C_{comp1}}$	
		$C_{comp2} = \frac{1}{2\pi \cdot f_{c2} \cdot R_{comp1} \cdot \tan(\Phi_{m2})}$	Φ_{m2} is the wished phase margin. It should be between 45° and 90°

9. as testified by the absence of the “dB” subscript label, the loop gains computed in this table are not in dB.

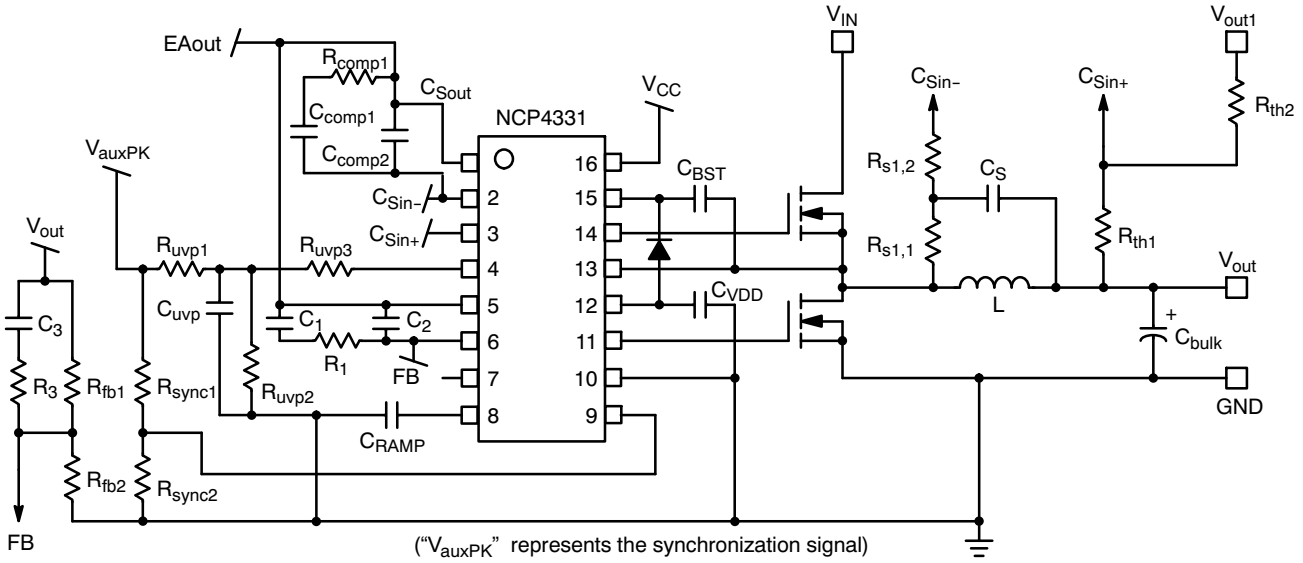

Figure 16. Generic Application Schematic

CONCLUSION

The NCP4331 represents a major leap towards an improved efficiency.

This application note proposes a systematic procedure to design a NCP4331−driven post regulator for an eased implementation.

For more information on the 3.3 V / 20 A application that illustrates the design process, please refer to application note AND8316/D at www.onsemi.com (under construction) that gives more practical details (BOM, PCB plots...) and performance data on the efficiency and the dynamic behavior.

A MathCad calculation file and an Excel Spreadsheet available at http://www.onsemi.com/PowerSolutions/product.do?id=NCP4331 automatically computes the calculations presented in this application note.

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